Micromachined Electro-Mechanically Tunable Capacitors and Their Applications to RF IC's

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***Abstract*—Micromachined electro-mechanically tunable capacitors with two and three parallel plates are presented. Experimental devices have been fabricated using a standard polysilicon surface micromachining process. The two-plate tunable capacitor has a measured nominal capacitance of 2.05 pF, a Q-factor of 20 at 1 GHz, and achieves a tuning range of 1.5 : 1. The three-plate version has a nominal capacitance of 4.0 pF, a Q-factor of 15.4 at 1 GHz, and a tuning range of 1.87 : 1. The tuning ranges achieved here are near theoretical limits. Effects due to various physical phenomena such as temperature, gravity, and shock are examined in detail. An RF voltage-controlled oscillator with an integrated inductor and a micromachined tunable capacitor is also demonstrated. The active circuit and the inductor have been fabricated in a 0.5-μm CMOS process. The voltage-controlled oscillator has been assembled by bonding together the CMOS and the micromachined parts. The 1.35-GHz voltage-controlled oscillator has a phase noise of -98.5 dBc/Hz at a 100 kHz offset from the carrier.**

***Index Terms*—Varactors, voltage-controlled oscillators.**

I. Introduction

MODERN communication systems such as the GSM cellular telephone system place stringent requirements on RF/IF filters and voltage-controlled oscillators (VCO's). Although much work has been done in the integration of a radio transceiver onto a single silicon chip [1], [2], many components such as band select, channel select, and tuning elements of the VCO must still remain external to the chip. It is difficult to integrate these elements onto a single chip, primarily because inductors and p-n junction varactors with high quality factors (Q-factor) are not available in standard silicon processes [3]–[5]. Low-noise RF VCO's require a resonant device with a high Q-factor, since the phase noise of an oscillator is proportional to $1/Q_T^2$ where Q_T is the overall Q-factor of the resonator [6]. High dynamic range filters also require a high Q-factor resonator, since the dynamic range of the filter is proportional to Q_T^2 [7].

Recent developments in micromachining suggest that technologies where micromachined devices and electronics reside on a single chip will be widely available in the future. Commercial products based on a BiCMOS technology with an integrated surface polysilicon process are already available today [8]. Such a technology makes possible realization of not only integrated mechanical resonant devices but also integrated electrical resonant circuits where one of the reactive elements is made tunable by electro-mechanical means.

Filters and oscillators based on mechanical resonant devices with a high Q-factor, which operate in the tens of megahertz, have already been demonstrated [9]–[11]. Although these devices are not suited for applications in the 1–2-GHz range, these devices may well find use in the intermediate frequency (IF) section of a radio transceiver. The mechanical resonant frequency, however, is not electronically tunable, since the resonant frequency is set by the proof mass and the equivalent spring constant of the suspension.

A tunable high Q-factor resonator, operating in the 1–2-GHz range, may be possible with an electrical resonant circuit where one of the reactive elements is electro-mechanically tunable. Micromachined electro-mechanically tunable capacitors have been shown to exhibit an adequate Q-factor when they are fabricated in either an aluminum [12] or a polysilicon [13] surface micromachining technology. A low phase noise 714-MHz CMOS VCO with a high Q-factor aluminum micromachined tunable capacitor and an off-chip inductor has also been recently demonstrated [14]. In addition, micromachined tunable capacitors are not expected to respond to RF frequencies in the 1–2-GHz range especially since their mechanical resonant frequencies normally lie in the 10–100 kHz. Therefore, with RF frequencies 10 000 times the mechanical bandwidth, these devices are unlikely to produce a significant amount of harmonic content. The main limitation of these devices, however, has been the fact that their tuning ranges thus far have been less than the theoretical calculations suggest [12], [13].

This paper presents two- and three-plate polysilicon micromachined tunable capacitors that have the largest tuning ranges reported to date. After the principle of their operation is described in Section II, the design issues including the computation of spring constants and Q-factors are discussed in Section III. In Section IV, detailed measurements of several devices are given. Many practical issues including the effect of temperature, humidity, gravity, and shock are examined in Section V. A VCO that uses a micromachined tunable capacitor is presented in Section VI before some conclusions are given in Section VII.

II. Principle of Operation

Fig. 1 shows a functional model of an electro-mechanically tunable capacitor that consists of two parallel plates. The top plate of the capacitor is suspended by a spring with spring constant k, while the bottom plate of the capacitor

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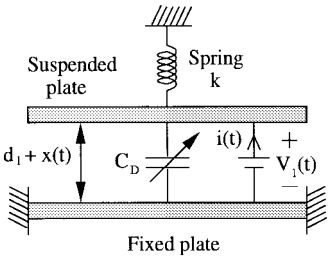

Fig. 1. Functional model of an electro-mechanically tunable parallel-plate capacitor with two parallel plates.

is mechanically secured. When a bias voltage $V_1(t) = V_1$ is applied across the capacitor plates, the suspended plate is attracted toward the bottom plate due to the resultant electrostatic force. The suspended plate moves toward the fixed plate until an equilibrium between the electrostatic and the spring forces is reached. Under dc conditions, $x(t) = x$, $V_1(t) = V_1$, and the equilibrium between the forces can be written mathematically as follows:

$$kx = \frac{1}{2}\frac{dC_D}{dx}V_1^2 = -\frac{1}{2}\frac{\epsilon_d A V_1^2}{(d_1+x)^2} \tag{1}$$

where ϵ_d is the dielectric constant of air ($\epsilon_d = \epsilon_{\text{air}}\epsilon_0$ where $\epsilon_{\text{air}} = 1.000\,54$ and $\epsilon_0 = 8.854\,15\times10^{-12}$ F/m), A is the area of the capacitor plates, and d_1 is the separation of the capacitor plates when the spring is in its relaxed state. Solving a cubic equation, an explicit expression for the desired capacitance $C_D(V_1)$ can be obtained [15] as follows:

$$\begin{aligned}
C_D(V_1) &= \frac{\epsilon_d A}{d_1 + x(V_1)} \\
x(V_1) &= (s_1(V_1) + s_2(V_1)) - \frac{2d_1}{3} \\
s_1(V_1) &= \left(w(V_1) + \sqrt{u^3 + w^2(V_1)}\right)^{1/3} \\
s_2(V_1) &= \left(w(V_1) - \sqrt{u^3 + w^2(V_1)}\right)^{1/3} \\
u &= \frac{d_1^2}{9} \\
w(V_1) &= \frac{d_1^3}{27} - \frac{\epsilon_d A V_1}{4k}.
\end{aligned} \tag{2}$$

It should be noted that an equilibrium between the spring and the electrostatic forces exists only for displacements $0 \geq x \geq -d_1/3$. The suspended plate will make contact with the bottom plate if the electrostatic force is greater than the spring force, which occurs when $x < -d_1/3$. The maximum capacitance that such a tunable capacitor can be tuned to is $3C_D/2$, and the maximum theoretical tuning range is $1.5:1$. Although the tunable capacitor is biased here using a voltage source, charge source can be used to control the amount of charges on the capacitor plates, in which case the equilibrium between the forces exists for $0 \geq x \geq -d_1$.

Fig. 2 shows a conceptual model of a three-plate electro-mechanically tunable capacitor where under zero bias condition the distances between parallel plates are d_1 and d_2, respectively. The top and bottom plates of the capacitor are fixed mechanically while the middle plate is suspended by

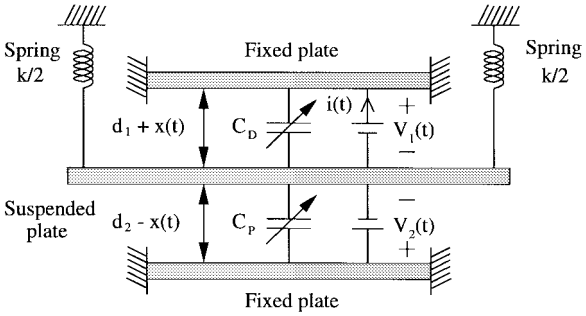

Fig. 2. Conceptual model of an electro-mechanically tunable parallel-plate capacitor with three parallel plates.

two springs with a spring constant $k/2$ each. If a bias voltage $V_1(t) = V_1$ is applied and $V_2(t) = 0$ V, the electrostatic force causes the suspended plate to move toward the top plate. Similarly, if a bias voltage $V_2(t) = V_2$ is applied and $V_1(t) = 0$ V, the suspended plate moves toward the bottom plate. Under dc conditions, $x(t) = x$, $V_1(t) = V_1$, $V_2(t) = V_2$, and the equilibrium between the electrostatic and the spring forces can be expressed as follows:

$$\begin{aligned}
kx &= \frac{1}{2}\frac{dC_D}{dx}V_1^2 + \frac{1}{2}\frac{dC_P}{dx}V_2^2 \\
&= -\frac{1}{2}\frac{\epsilon_d A V_1^2}{(d_1+x)^2} + \frac{1}{2}\frac{\epsilon_d A V_2^2}{(d_2-x)^2}.
\end{aligned} \tag{3}$$

The maximum capacitance that this capacitor can be tuned to is still $3C_D/2$. However, the minimum capacitance that this capacitor can be tuned to is $3C_D/4$, if distances d_1 and d_2 are equal. Hence, the maximum theoretical tuning range is $2:1$. Note that in a practical circuit application, the middle plate of the tunable capacitor must be connected to a small-signal ground so that only the desired capacitance C_D plays a role in the actual circuit.

The dynamics of an electro-mechanical system such as the one in Fig. 1 can be described as follows:

$$m\frac{d^2x(t)}{dt^2} + r\frac{dx(t)}{dt} + kx(t) = \frac{1}{2}\frac{dC_D(t)}{dx}V_1^2(t) \tag{4}$$

where m is the mass of the suspended plate and r is the mechanical resistance. The current flowing through the desired capacitance C_D is given by

$$i(t) = C_D(t)\frac{dV_1(t)}{dt} + V_1(t)\frac{dC_D(t)}{dt}. \tag{5}$$

Equations (4) and (5) above have been implemented in HSPICE, a standard circuit simulator. The equivalent circuit model of the electro-mechanical tunable capacitor with two parallel plates is shown in Fig. 3. Although in typical implementations of SPICE it is not possible to implement signal sources with arbitrary nonlinearities, the nonlinear and signal dependent current and voltage sources can be implemented in HSPICE with relative ease. Note that the model in Fig. 3 preserves noise properties of the mechanical system. In addition, the magnitudes of the force and the displacement have to be carefully scaled in order to avoid numerical problems. The model finds use in simulation of circuits which employ the electro-mechanical components that can be modeled by Fig. 3.

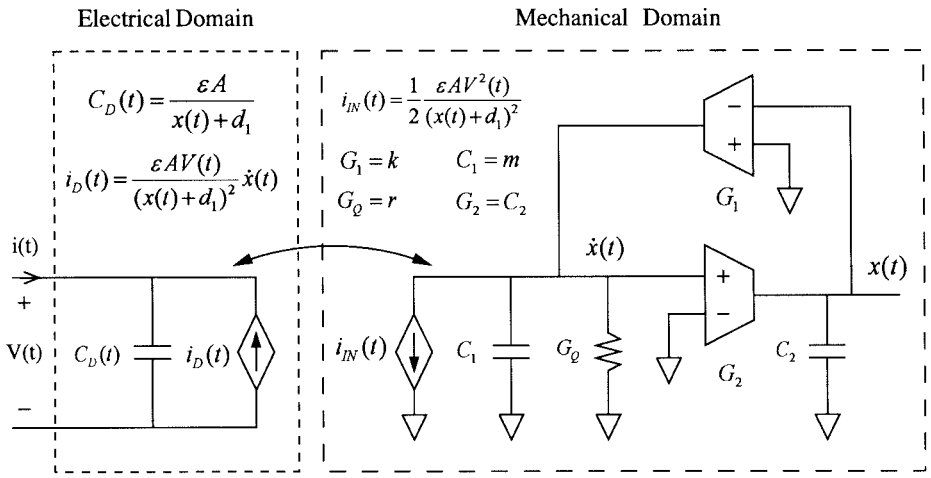

Fig. 3. SPICE model of an electro-mechanically tunable capacitor.

TABLE I
SUMMARY OF SELECTED MUMP'S PROCESS PARAMETERS

Layer	*Thickness*	*Sheet Resistance*
Poly0	0.5 μm	30 Ω/sq
Poly1	2.0 μm	10 Ω/sq
Poly2	1.5 μm	20 Ω/sq
Gold	0.5 μm	0.06 Ω/sq

III. DESIGN OF MICROMACHINED TUNABLE CAPACITORS

Despite the superior electrical properties of aluminum, polysilicon was chosen as the structural material for tunable capacitors due to its good mechanical properties [16]. Several electro-mechanically tunable capacitors with two and three parallel plates have been designed in a standard polysilicon surface micromachining process (MUMP's) [17]. The process features three layers of polysilicon (poly0, poly1, and poly2) and one layer of gold (gold can only be deposited on poly2). Selected MUMP's process parameters are summarized in Table I.

MUMP's devices are released using an HF sacrificial layer etch and a supercritical carbon dioxide drying process [17]. Micromachined tunable capacitors that are released using an HF etch and conventional drying methods may suffer from a stiction problem which can result in an unsatisfactory device yield. During the drying process, attractive capillary forces can bring the capacitor plates into permanent contact, effectively shorting the tunable capacitor permanently [18]. The supercritical carbon dioxide drying process alleviates the stiction problem and dramatically improves device yield [19].

A. Tunable Capacitor Design

Fig. 4 shows the simplified top and cross-section views of a 0.6-pF tunable capacitor with two parallel plates. Poly1 and poly2/gold layers were selected as capacitor plates, since in the MUMP's process poly1 and poly2/gold layers are the most conductive layers (see Table I). Given the air gap of 0.75 μm (after sacrificial layer release), the desired capacitance can be achieved with a 210 $\times$ 230 μm plate area. A spring

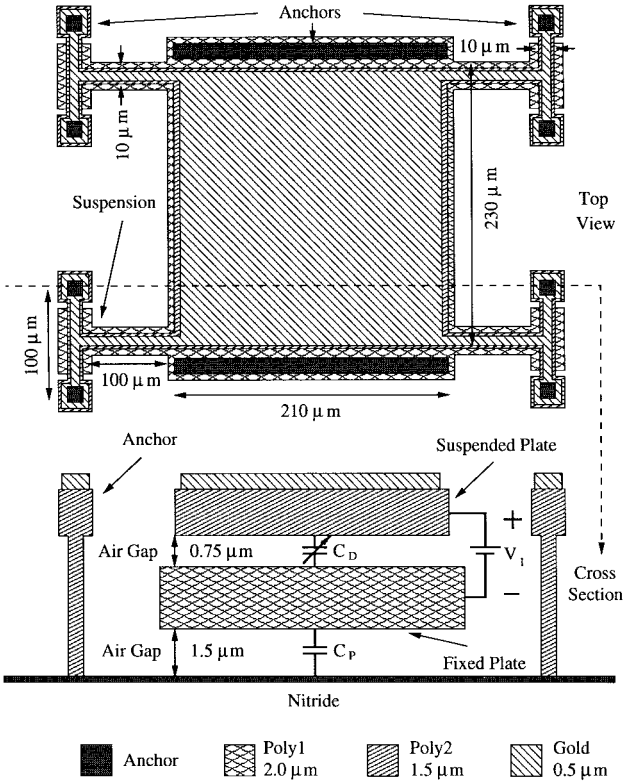

Fig. 4. Simplified top and cross-section views of a two-plate micromachined tunable capacitor (0.6 pF design value).

constant of 37.2 N/m is necessary in order to achieve a maximum capacitance of 0.9 pF under the maximum bias voltage of $V_1 = 3.3$ V. The mass of the suspended plate, which is composed of the poly2/gold layers, is 0.6 μg, and the mechanical resonant frequency is estimated to be 39 kHz.

A 1.0-pF tunable capacitor has also been designed. The required capacitance can be obtained with 295 $\times$ 295 μm plates, given the air gap of 0.75 μm. In order to achieve a maximum capacitance of 1.5 pF when $V_1 = 3.3$ V, a spring constant of 65.3 N/m is required. The mechanical resonant frequency is estimated at 38.8 kHz, while the mass of the poly2/gold suspended plate is 1.1 μg.

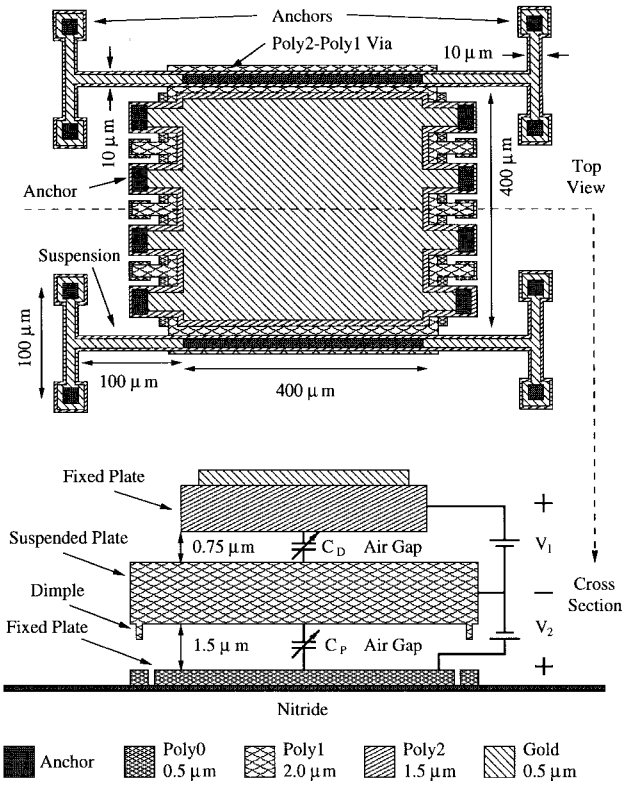

Fig. 5. Simplified top and cross-section views of a three-plate micromachined tunable capacitor (1.9 pF design value).

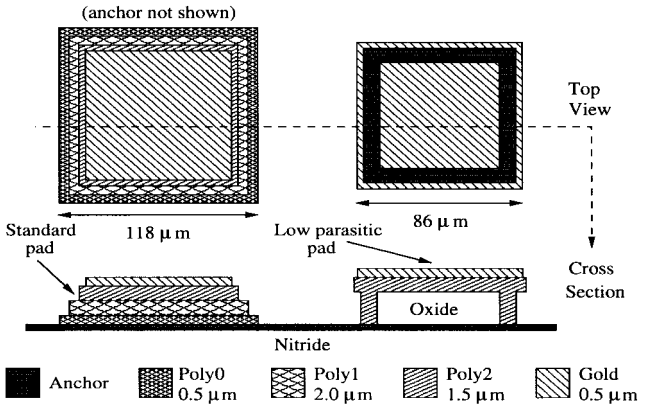

Fig. 6. Simplified top and cross-section views of a conventional (1.5 pF) and a low parasitic (0.25 pF) pad in MUMP's process.

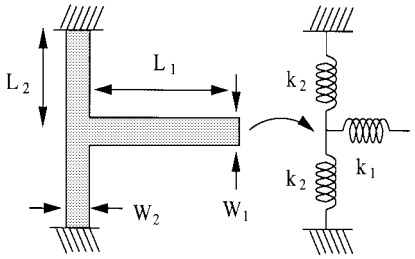

Fig. 7. Simplified diagram and a spring model of the T-type suspension.

Fig. 5 shows the top and the cross-section views of a 1.9-pF tunable capacitor, which consists of three parallel plates. A capacitor with an air gap of 0.75 μm and a 398 $\times$ 398 μm plate area achieves the desired capacitance. A spring constant of 122 N/m is necessary in order to obtain a maximum capacitance of 2.85 pF when $V_1 = 3.3$ V and $V_2 = 0$ V. The mass of the suspended plate, which is composed of poly1 layer, is then 0.7 μg, and the mechanical resonant frequency is estimated at 65.8 kHz. Dimples are used to prevent the middle plate (poly1) from sticking to the bottom plate (poly0) in the presence of excessive bias voltage V_2.

B. Pad Design

The parasitic capacitance of the pads is extremely critical, especially since die bonding and flip-chip technology are often used to integrate active circuits with micromachined devices. The standard pad in the MUMP's process has a parasitic capacitance of 1.5 pF, which significantly limits the tuning range. Therefore, a low parasitic pad, which has a parasitic capacitance of only 0.25 pF (Fig. 6), has been developed. A smaller capacitance per area is achieved by the use of only poly2 and gold layers, which are deposited on 2.25-μm thick oxide prior to sacrificial layer release. To protect the oxide underneath the pad from HF etch, anchors are placed around the edges of the pad. In addition, a smaller pad (86 $\times$ 86 μm) is used.

C. Suspension Design

Fig. 7 shows a conceptual diagram of the T-type suspension which is used in the design of tunable capacitors. The equivalent spring constant of this suspension can be approximately modeled as a parallel and series combination of springs as follows:

$$k_{eq} = \frac{k_1 2k_2}{k_1 + 2k_2}. \tag{6}$$

The stiffness constant for a double-clamped suspension beam may be used, if the capacitor plate is assumed to be rigid. The stiffness constant is given by

$$k_i = \frac{E_{\text{poly}} W_i T_i^3}{L_i^3} \tag{7}$$

where W_i, T_i, L_i are the width, thickness, and length of the beam, respectively, and E_{poly} is the Young's modulus (approximately 160 GPa) of polysilicon [20]. Since the overall suspension consists of four such beam arrangements, the total spring constant is $k_{\text{tot}} = 4k_{eq}$. Since the RF signal passes through the suspension beams, gold is deposited on top of the suspension beams in order to minimize series losses. Deposition of gold on suspension beams is not expected to have significant effect on the overall spring constant because the gold trace has a smaller width and thickness relative to the polysilicon beam. Furthermore, the Young's modulus of gold is 50% lower than that of polysilicon (approximately 80 GPa).

D. Q-Factor of the Polysilicon Tunable Capacitor

Q-factor is an important characteristic of a tunable capacitor in many RF applications. The top plate of tunable capacitors is implemented using poly2/gold layers, which provide a low resistance. However, the bottom plate of the two-plate and the middle plate of the three-plate tunable capacitors are composed

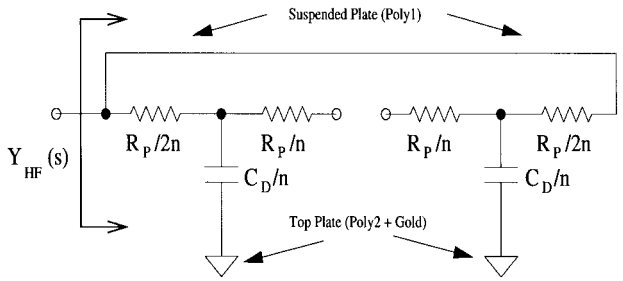

Fig. 8. Distributed *RC* model of the proposed polysilicon micromachined tunable capacitor.

of poly1 which has rather high sheet resistance. In order to evaluate the effect of the poly1 plate on the Q-factor, the tunable capacitor is modeled as a distributed *RC* line (Fig. 8), where the poly2/gold plate is assumed to be equipotential. The input admittance to such a distributed *RC* line is given by

$$Y_{hf}(s) = \frac{\sqrt{s\tau}}{R_P}\frac{\sinh\sqrt{s\tau}}{1+\cosh\sqrt{s\tau}} \quad \text{and} \quad \tau = R_P C_D \tag{8}$$

where R_P is the resistance of the poly1 plate and C_D is the desired capacitance. From (8), an expression for the Q-factor can be obtained

$$\frac{Q+1}{Q-1} = \frac{\sin\left(\sqrt{2\omega\tau}\right) + 2\cosh\left(\sqrt{\frac{\omega\tau}{2}}\right)\sin\left(\sqrt{\frac{\omega\tau}{2}}\right)}{\sinh\left(\sqrt{2\omega\tau}\right) + 2\sinh\left(\sqrt{\frac{\omega\tau}{2}}\right)\cos\left(\sqrt{\frac{\omega\tau}{2}}\right)}. \tag{9}$$

The expression derived above represents the maximum theoretically achievable Q-factor, since losses due to the interconnect are not considered. At 1 GHz, the calculated Q-factors for 0.6, 1.0, and 1.9 pF tunable capacitors are 318, 191, and 95, respectively, which suggests that a high Q-factor can be achieved in a MUMP's process. The Q-factor estimate is lower, however, when the series interconnect resistance is considered, in particular the resistance of the poly1–poly2 via and the resistance of the deposited gold on the suspension beam. With interconnect resistance considered, the Q-factors are estimated at 84.8, 55.2, and 26.6, at 1 GHz, for 0.6, 1.0, and 1.9 pF tunable capacitors, respectively.

IV. Measurement Results

All measurements were done using an HP 8753D network analyzer, a Cascade probe station, and WinCal software. *The measurements include the parasitic capacitances of the pads.* An open pad measurement indicates a pad-to-substrate capacitance of approximately 0.26 pF.

Fig. 9 shows a microphotograph of the tunable capacitor with two parallel plates (210 × 230 μm capacitor). The capacitor has a Q-factor of 20 at 1 GHz and Q-factor of 11.6 at 2 GHz (Fig. 10). The self-resonant frequency is beyond 6 GHz, the maximum operating frequency of the HP 8753D network analyzer. The tuning characteristics of the tunable capacitor are shown in Fig. 11. When a zero bias voltage ($V_1 = 0$ V) is applied, the measured capacitance is 2.05 pF. The measured capacitance is 3.1 pF when $V_1 = 4$ V is applied.

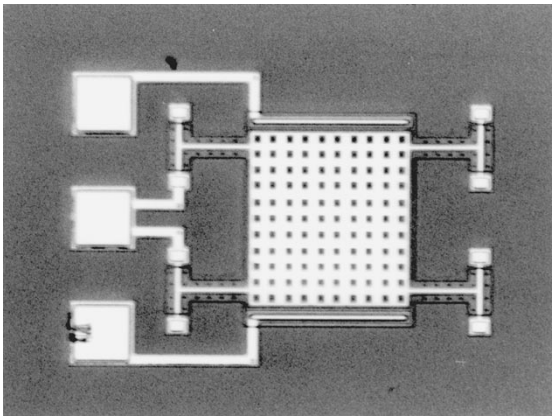

Fig. 9. Microphotograph of a two-plate tunable capacitor (0.6 pF design value).

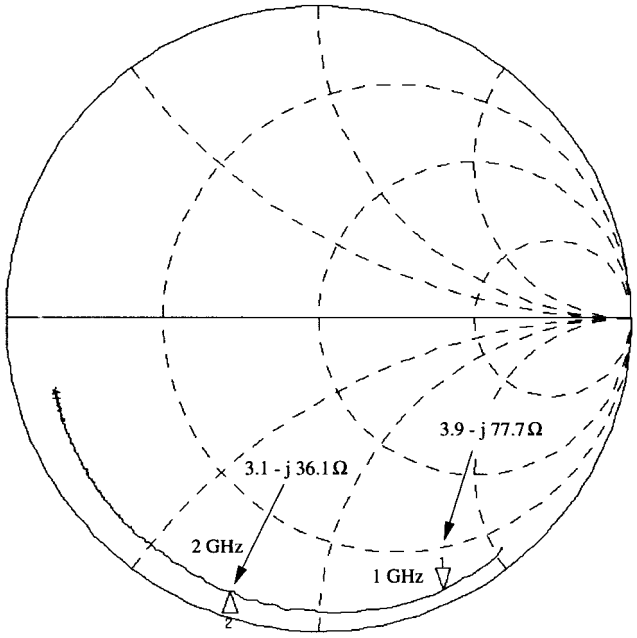

Fig. 10. Measured S_{11} of the two-plate tunable capacitor (0.6 pF design value).

The tuning range of the micromachined tunable capacitor is hence 1.5 : 1. Statistics show that the average measured nominal capacitance is 1.98 pF and the standard deviation is 0.14 pF using the data from 14 functional devices (16 devices were fabricated).

The fabricated micromachined tunable capacitor with three parallel plates (400 × 400 μm capacitor) is shown in Fig. 12. The tunable capacitor has a measured Q-factor of 15.4 at 1 GHz and 7.1 at 2 GHz (Fig. 13). The self-resonant frequency is approximately 6 GHz. Fig. 14 shows the tuning characteristics of the tunable capacitor. Under zero bias conditions (i.e., $V_1 = 0$ V and $V_2 = 0$ V), the measured capacitance (i.e., the desired capacitance C_D) is 4.0 pF. The measured capacitance is approximately 6.4 pF when $V_1 = 1.8$ V and $V_2 = 0$ V are applied. When $V_1 = 0$ V and $V_2 = 4.4$ V are set, the measured capacitance is 3.4 pF. The tunable capacitor hence has a tuning range of 1.87 : 1. If the V_2 is more than 4.4 V while $V_1 = 0$ V, bistability and discontinuity in tuning are observed.

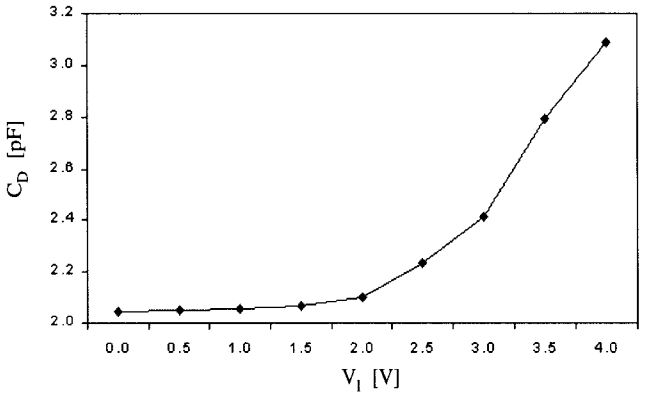

Fig. 11. Measured tuning characteristics of the two-plate tunable capacitor (0.6 pF design value).

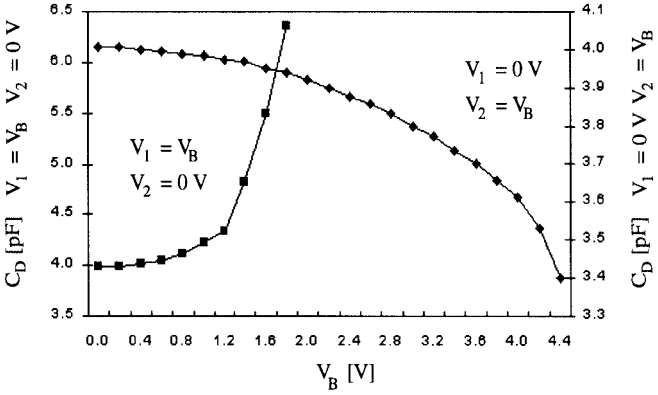

Fig. 14. Measured tuning characteristics of the three-plate tunable capacitor (1.9 pF design value).

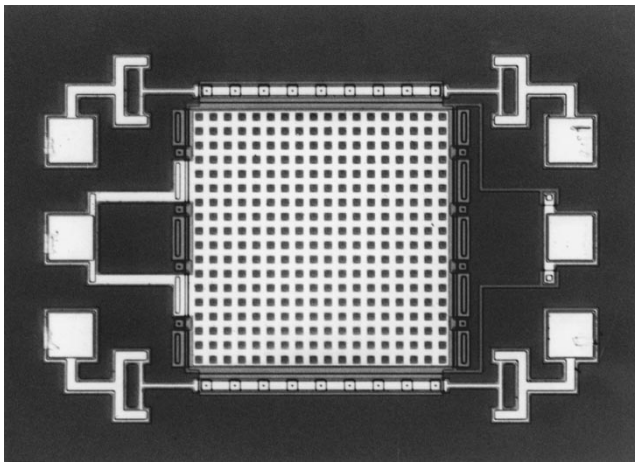

Fig. 12. Microphotograph of a three-plate tunable capacitor (1.9 pF design value).

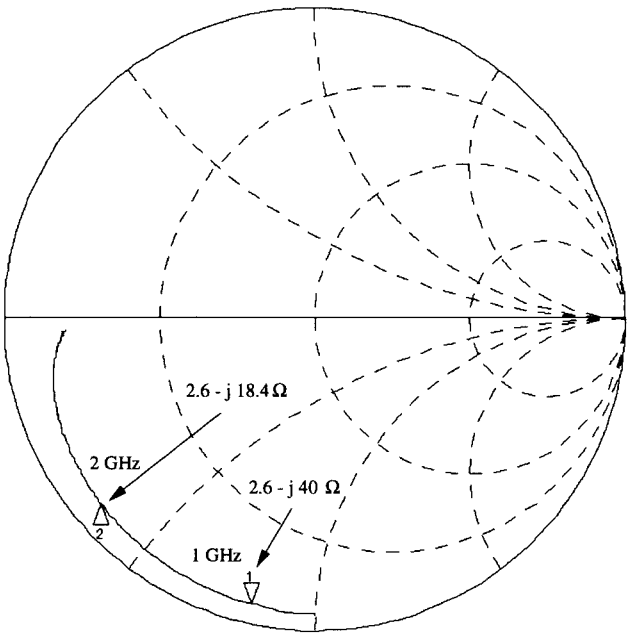

Fig. 13. Measured S_{11} of the three-plate tunable capacitor (1.9 pF design value).

TABLE II
SUMMARY OF MICROMACHINED TUNABLE CAPACITOR MEASUREMENTS

Varactor Type	*Two-plate*	*Two-plate*	*Three-plate*
Plate Area	210 μm × 230 μm	295 μm × 295 μm	400 μm × 400 μm
Designed Capacitance	0.6 pF	1.0 pF	1.9 pF
Measured Capacitance	2.05 pF	3.26 pF	4.0 pF
Measured Q-factor	20.0	13.6	15.4
Tuning Range	1.5:1	1.5:1	1.87:1
Tuning Voltages	0 - 4 V	0 - 3.5 V	0 - 1.8 V 0 - 4.4 V
Fabricated Devices	16	16	96
Nonfunctional Devices	2	1	7
Average Capacitance	1.98 pF	3.39 pF	3.63 pF
Standard Deviation	0.14 pF	0.28 pF	0.52 pF

The capacitance suddenly drops to approximately 2.2 pF and returns to 2.3 pF when the bias voltages are set back to 0 V. The capacitor is still tunable, but the tuning range in this mode is only 1.12 : 1. The device returns to the previous mode (i.e., 4.0 pF nominal capacitance), provided $V_1 = 5.0$ V and $V_2 = 0$ V are applied before the bias voltages are reset to 0 V. Out of the 96 fabricated devices, seven tunable capacitors were not functional. The average measured nominal capacitance was 3.63 pF and the standard deviation was 0.52 pF.

The measured results for 210 × 230 μm and 295 × 295 μm two-plate capacitors, and a 400 × 400 μm three-plate capacitor are summarized in Table. II. Although further statistical data is necessary, this preliminary data seems to indicate that the tuning range of micromachined tunable capacitors is wide enough to cover process variations.

Micromachined two-plate tunable capacitors have been tested from −10 °C to 100 °C. The devices were functional over the temperature range, but their tuning characteristics changed as the poly silicon and gold characteristics changed with temperature. The tunable capacitor with two parallel plates (0.6 pF design value) has a temperature coefficient of 2050 ppm/°C. At high temperatures, the stiffness coefficient of the suspension decreases, and consequently a lower control voltage is required to achieve the 1.5 : 1 tuning range.

A 100-Hz 3-V square-wave was applied across the tunable capacitor with two parallel plates (295 × 295 μm capacitor) in order to test the reliability of a micromachined tunable

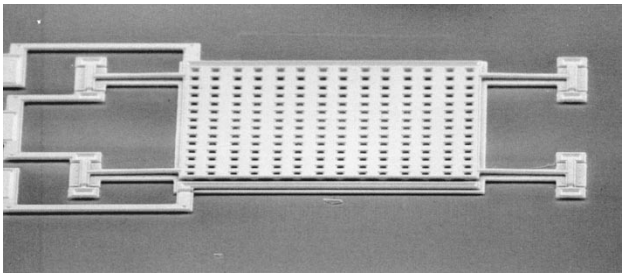

Fig. 15. SEM photograph of the two-plate tunable capacitor (1.0 pF design value).

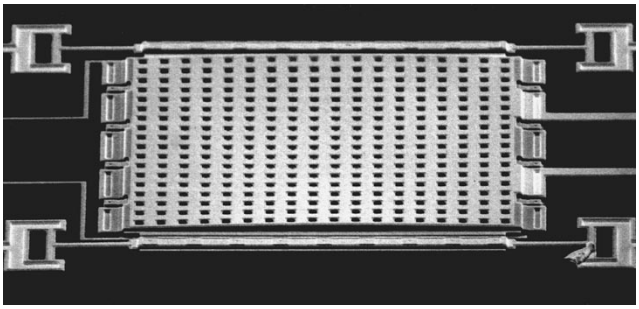

Fig. 16. SEM photograph of the three-plate tunable capacitor (1.9 pF design value).

capacitor. No change in tunable capacitor characteristics has been observed even after 120 million cycles (i.e., two weeks).

V. Discussion

A. Residual Stress

The measured capacitances of the experimental devices are significantly larger than the designed values. Parasitic capacitance to the substrate adds approximately 0.37, 0.4, and 0.6 pF to the overall designed capacitance of the 0.57, 1.0, and 2.0 pF tunable capacitors, respectively. Furthermore, residual stress in the polysilicon plates produces warping of the capacitor plates, which effectively results in a different capacitor plate separation and, thus, a different parallel-plate capacitance [21].

Fig. 15 shows an SEM photograph of a two-plate tunable capacitor (1.0 pF design value). A small upward displacement of suspension beams is clearly visible. Although the top plate does not appear to be warped, the low-magnification microphotographs indicate some downward warping. The shape of the bottom plate cannot be observed.

The SEM photograph of a tunable capacitor with three parallel plates (1.9 pF design value) is shown in Fig. 16. From the photograph, it is clear that the top plate is warped upward. It is difficult to evaluate the shape of the middle plate from the photograph. The shape of the bottom plate does not change upon sacrificial layer release since it is directly deposited on the nitride.

It is believed that the bistability observed in the three-plate tunable capacitor is due to the warping of the top or the middle plate, since the direction of plate warping (i.e., upward or downward) can be changed with an application of appropriate dc voltages.

Structures with low residual stress are being investigated to minimize warping and bistability so that the tuning range of three-plate tunable capacitors can be further improved.

B. Q-Factor

The Q-factor values for the experimental devices fall short of their theoretical estimates. While the Q-factor of a micromachined tunable capacitor is limited by the series resistance of the interconnect, the measured capacitance is higher than the designed value, and hence a lower Q-factor is measured. Taking the measured nominal capacitances into account, the Q-factors are estimated at 25.5, 17.2, and 16.5 for 2.05, 3.2, and 4.0 pF (i.e., 0.6, 1.0, and 1.9 pF design values) tunable capacitors, respectively.

The skin-effect is not a problem since the skin depth of gold is 2.4 μm at 1 GHz and 1.7 μm at 2 GHz (given 0.5-μm thick gold). However, since MUMP's process is not a planarized process, steps in gold interconnect can result in a high interconnect resistance [17]. Though MUMP's is not a planarized process, surface micromachining technologies that use a chemical-mechanical polishing process to achieve layer planarization are available [22].

Since the Q-factor of the micromachined tunable capacitor is limited by the series interconnect, alternative suspension designs that can provide the desired spring constant and yet have a low series resistance will be investigated in the future. In addition, future designs will use wider interconnect in order to increase the Q-factor even further.

C. Effects Due to Ambient Conditions

Since air is used as a dielectric for the tunable capacitor, its properties as a function of pressure, temperature, and humidity must be examined. An empirical expression for the dielectric constant of air as a function of pressure and temperature is shown below:

$$\epsilon_{\text{air}}(P, T) = 1 + 0.157\frac{P}{T} \tag{10}$$

where P is the pressure in atm and T is the absolute temperature in kelvin [23]. Under the normal atmospheric conditions (i.e., 293 K and 1 atm), the dielectric constant of air has a temperature coefficient of -2 ppm/K when humidity is 0% and 10 ppm/K when humidity is 100% [24]. It is apparent from (10) that practical variations in atmospheric conditions have a small effect on the dielectric constant of air and hence on the capacitance.

Under normal atmospheric conditions, the dielectric strength of air is only 0.8 kV/mm [24], which suggests that arcing between capacitor plates may be present. Further examinations, however, show that the dielectric breakdown field of air is a nonlinear function of electrode spacing [25]. For instance, under the normal atmospheric conditions, the breakdown field of air is 4.5 kV/mm for a 1-mm air gap (breakdown voltage of 4.5 kV) and 12.5 kV/mm for a 0.06-mm air gap (breakdown voltage of 750 V).

The tunable capacitor may be operated in vacuum, which resolves many issues that can arise when air is used as a dielectric. For example, the mechanical resistance r can be dramatically reduced, and hence the mechanical Q-factor can be significantly improved when the tunable capacitor is placed in vacuum. In addition, the mechanical noise due to the thermal agitation of air molecules can be reduced as mechanical resistance r is reduced. Furthermore, there is no dielectric breakdown in vacuum. However, specialized packaging is needed to ensure vacuum.

Although temperature has a small effect on the dielectric constant of air, the thermal expansion of polysilicon and gold layers results in the deformation of capacitor plates and, hence, significant capacitance change. The thermal expansion of a material is often given by

$$\Delta L = \alpha L \Delta T \tag{11}$$

where α is the linear expansion coefficient, ΔT is the temperature change in degrees kelvin, L is length in meters, and ΔL is the increase in length due to the thermal expansion in meters. The thermal coefficient of expansion α is 2.6 ppm/K for silicon and 14 ppm/K for gold [26]. For example, a 295 $\times$ 295 μm poly1 plate expands by 0.07 μm, given a 100° change in temperature, while a gold plate with the same dimensions expands by 0.38 μm.

D. Effects Due to Motion

In order to evaluate the effect of gravity on the micromachined tunable capacitor, the displacement x_g should be calculated as follows:

$$x_g = \frac{mg}{k} \tag{12}$$

where g is the gravity ($g = 9.80665$ m/s^2). For example, the 0.6 pF capacitance would change by approximately 0.02% due to the gravitational pull on the suspended plate. Conversely, an acceleration of approximately 432 g is required in order to observe a 10% change in the capacitance value.

An important consideration when dealing with micromachined devices is the ability of the devices to survive shock. Several devices have been dropped accidentally from approximately 2.5 ft and have been found to function properly after the drop.

In order to ensure the proper release of the micromachined tunable capacitor, sufficient number of etch holes must be placed across the capacitor plates. Although the mechanical strength of the polysilicon plate is reduced, the reduction of the effective Young's modulus is only 18% [27].

VI. An Application: VCO

Fig. 17 shows a circuit schematic of a CMOS VCO with an on-chip spiral inductor and an off-chip three-plate micromachined tunable capacitor. The CMOS oscillator consists of a source follower M_2 driving a common gate amplifier M_1. The bias current is supplied by transistors M_3 and M_4. The LC tank is formed by an on-chip inductor and a micromachined tunable capacitor. The inductor and the tunable capacitor are bonded

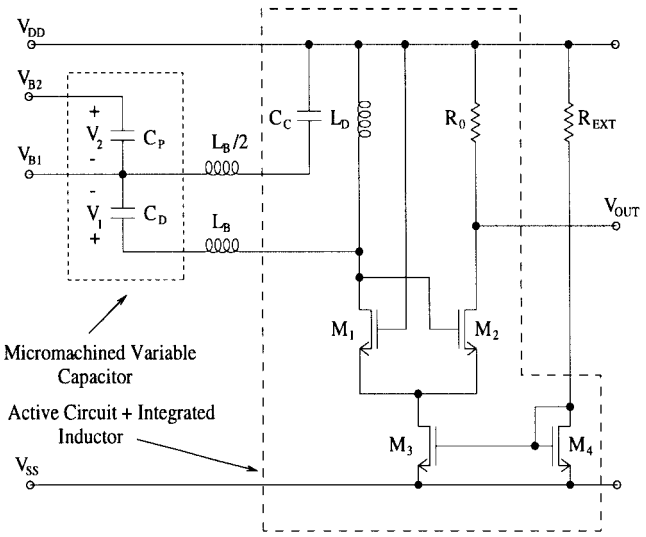

Fig. 17. Circuit schematic of a CMOS VCO with an integrated inductor and a micromachined tunable capacitor as a tuning element.

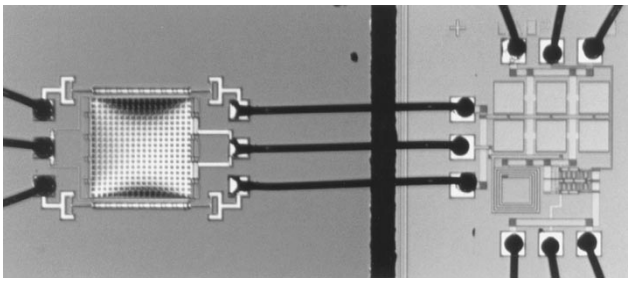

Fig. 18. Microphotograph of the experimental VCO: MUMP's (left) and MOSIS (right) dice bonded together.

together where the effect of bonding is shown by inductors L_B and $L_B/2$. The oscillations start provided that, at resonance, the loop gain is greater than unity (i.e., $\frac{1}{2}\, g_{m1,2} Q_L \omega_0 L > 1$). The oscillator output is taken from the drain of M_2, which isolates the LC tank from the load. A pull-up resistance R_0 of 50 Ω is used to accommodate the RF measurement equipment, and an on-chip bypass capacitor C_C of 6 pF is used to ensure that the parasitic capacitance C_P does not affect the LC tank.

The active circuit and the on-chip inductor were fabricated in an HP 0.5-μm CMOS (MOSIS) process. The microphotograph of the VCO is shown in Fig. 18. The micromachined tunable capacitor (left) and the CMOS circuit (right) were bonded together using a manual ball-wedge bonding machine. Each bonding wire is approximately 1 mm long, which corresponds to series inductance L_B of 1 nH. The integrated inductor L_D has a measured inductance of 4 nH and a Q-factor of 1.8 at 1.35 GHz.

All measurements were done in a quad flat-pack ceramic package on an FR4 test board. The output spectrum of the VCO is shown in Fig. 19. The carrier-to-noise ratio of the VCO is -98.5 dBc/Hz at a 100-kHz offset from the 1.35-GHz carrier, which is limited the Q-factor of the on-chip inductor. The circuit delivers -3.34 dBm of power into a 50-Ω load, while the oscillation frequency is tunable from 1336–1360 MHz. The VCO consumes 60 mW from a 3.3-V power supply.

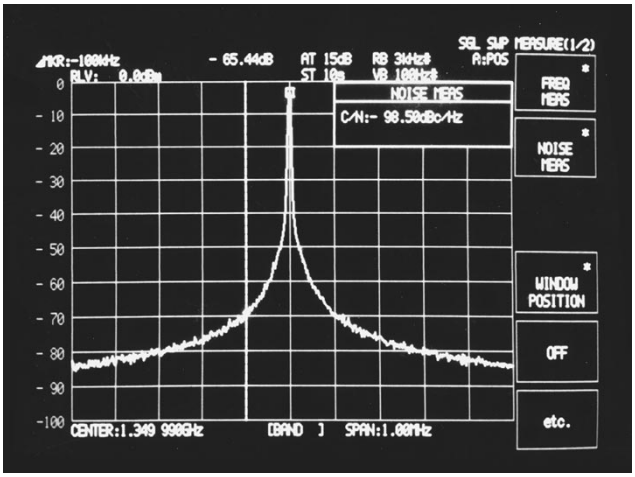

Fig. 19. Measured output spectrum of the VCO.

The three-plate tunable capacitor (1.9 pF designed value) operated in a second bistable mode where the desired capacitance is tunable from 2.2–2.3 pF. The measured tuning range is hence very low. When the capacitance operated in the first bistable mode where the capacitance is tunable from 3.4–6.4 pF, the VCO failed to oscillate at the desired frequency, and parasitic 5-GHz oscillations due to the bonding wire inductance were observed. This is expected since the nominal capacitance is very far from the designed value of 1.9 pF.

VII. Conclusion

Micromachined electro-mechanically tunable capacitors, fabricated in a standard polysilicon surface micromachining process, have been demonstrated. Even though polysilicon was used as the structural material, theoretical calculations show that tunable capacitors with relatively high Q-factors are possible. In addition, experimental devices achieve tuning ranges which are near theoretical limits. The two-plate tunable capacitor has a nominal capacitance of 2.05 pF, 1.5 : 1 tuning range with 4.0 V bias voltage, and a Q-factor of 20 at 1 GHz. The three-plate device has a nominal capacitance of 4.0 pF, 1.87 : 1 tuning range with 4.4 V bias voltage, and Q-factor of 15.4 at 1 GHz. No changes in the two-plate device characteristics due to wear have been observed even after 120 million cycles. The two-plate tunable capacitor was also found to be functional over -10 °C to 100 °C temperature range. Moreover, dependence of various physical phenomena such as as temperature, pressure, humidity, and shock on capacitor characteristics has been discussed. A voltage-controlled oscillator with an integrated inductor and a micromachined three-plate tunable capacitor has been also demonstrated. The active circuits and the inductor have been fabricated using a 0.5-μm CMOS process. The micromachined tunable capacitor and active circuits have been bonded together to produce the VCO. The 1.35-GHz VCO has a phase noise of -98.5 dBc/Hz, which is primarily limited by the low Q-factor of the on-chip inductor. Future work includes the design of micromachined tunable capacitors with higher Q-factors as well as the design of a tunable RF CMOS amplifier.

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References

[1] P. Gray and R. Meyer, "Future directions in silicon IC's for RF personal communications," in *IEEE Proc. CICC*, May 1995, pp. 83–90.
[2] A. Abidi, A. Rofougaran, G. Chang, J. Rael, J. Chang, M. Rofougaran, and P. Chang, "The future of CMOS wireless transceivers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1997, pp. 118–119.
[3] N. Nguyen and R. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1028–1031, Aug. 1990.
[4] J. Burghartz, K. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," *IEEE Electron Device Lett.*, vol. 17, pp. 428–430, Sept. 1996.
[5] M. Soyuer, K. Jenkins, J. Burghartz, and M. Hulvey, "A 3 V 4 GHz nMOS voltage-controlled oscillator with integrated resonator," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 394–395.
[6] W. P. Robins, *Phase Noise in Signal Sources: Theory and Applications.* Stevenage, U.K.: Peregrinus, 1982, pp. 49–53.
[7] S. Pipilos, Y. P. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC filter with tunable center frequency and quality factor," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1517–1525, Oct. 1996.
[8] K. H. Chau, S. R. Lewis, Y. Zhao, R. T. Howe, S. F. Bart, and R. G. Marcheselli, "An integrated force-balanced capacitive accelerometer for low-g applications," in *Proc. Int. Conf. Solid-State Sensors and Actuators and Eurosensors IX*, vol. 1, June 1995, pp. 593–596.
[9] T. Nguyen and R. Howe, "CMOS micromechanical resonator oscillator," in *IEEE IEDM Dig. Tech. Papers*, 1993, pp. 199–202.
[10] T. Nguyen, "Micromechanical resonators for oscillators and filters," in *IEEE Proc. Ultrasonics Symp.*, 1995, pp. 489–499.
[11] ——, "High-Q micromechanical oscillators and filters for communications," in *IEEE Proc. ISCAS*, May 1997, pp. 489–499.
[12] D. J. Young and B. E. Boser, "A micromachined variable capacitor for monolithic low-noise VCO's," in *IEEE Solid-State Sensor and Actuator Workshop Dig.*, June 1996, pp. 86–89.
[13] A. Dec and K. Suyama, "Micromachined varactor with a wide tuning range," *Electron. Lett.*, vol. 33, no. 11, pp. 922–924, May 1997.
[14] D. J. Young and B. E. Boser, "A micromachined-based RF low-noise voltage-controlled oscillator," in *IEEE Proc. CICC*, May 1997, pp. 431–434.
[15] M. Abramowitz and A. Stegun, *Handbook of Mathematical Functions with Formulas, Graphs, and Mathematical Tables.* New York: Dover, 1972.
[16] K. E. Petersen, "Silicon as a mechanical material," *Proc. IEEE*, vol. 70, pp. 420–457, May 1982.
[17] D. A. Koester, R. Mahadevan, A. Shishkoff, and K. W. Markus, "SmartMUMP's design handbook including MUMP's introduction and design rules," *MEMS Technology Applications Center*, July 1996, pp. 1–8.
[18] R. Legtenberg, A. C. Tilmans, J. Elders, and M. Elwenspoek, "Stiction of surface micromachined structures after rinsing and drying: Model and investigation of adhesion mechanisms," *Sensors and Actuators A*, pp. 230–238, 1994.
[19] C. W. Dyck, J. H. Smith, S. L. Miller, E. M. Russick, and C. L. Adkins, "Supercritical carbon dioxide solvent extraction from surface micromachined micromechanical structures," *Proc. SPIE*, pp. 225–235, Oct. 1996.
[20] E. Peeters, "Silicon accelerometers: Generic design and operating principles and a case study," *Proc. SPIE*, vol. 2882, pp. 134–146, Oct. 1996.
[21] G. X. Li and R. J Gutteridge, "Stress-induced warpage and the compensation in a composite micro-accelerometer," *Proc. SPIE*, vol. 2882, pp. 147–151, 1996.
[22] J. J. Sniegowski "Chemical-mechanical polishing: Enhancing the manufacturability of MEMS," *Proc. SPIE*, vol. 2879, pp. 104–150, Oct.

1996.
[23] B. H. Billings, D. F. Bleil, R. K Cook, H. M. Crosswhite, H. P. Frederikse, R. B. Lindsay, J. B. Marion, and M. W. Zemansky, *American Institute of Physics Handbook.* New York: McGraw-Hill, 1963.
[24] A. D. Khazan, *Transducers and Their Elements: Design and Application.* Englewood Cliffs, NJ: PTR Prentice Hall, 1993.
[25] I. S. Grigoriev and E. Z. Meilikhov, *Handbook of Physical Quantities.* Boca Raton, FL: CRC Press, 1997.
[26] J. W. Gardner, *Microsensors: Principles and Applications.* New York: Wiley, 1995.
[27] W. N. Sharpe, R. Vaidyanathan, B. Yuan, G. Bao, and R. L. Edwards, "Effect of etch holes on the mechanical properties of polysilicon," *J. Vac. Sci. Technol.*, pp. 1599–1603, Oct. 1997.

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